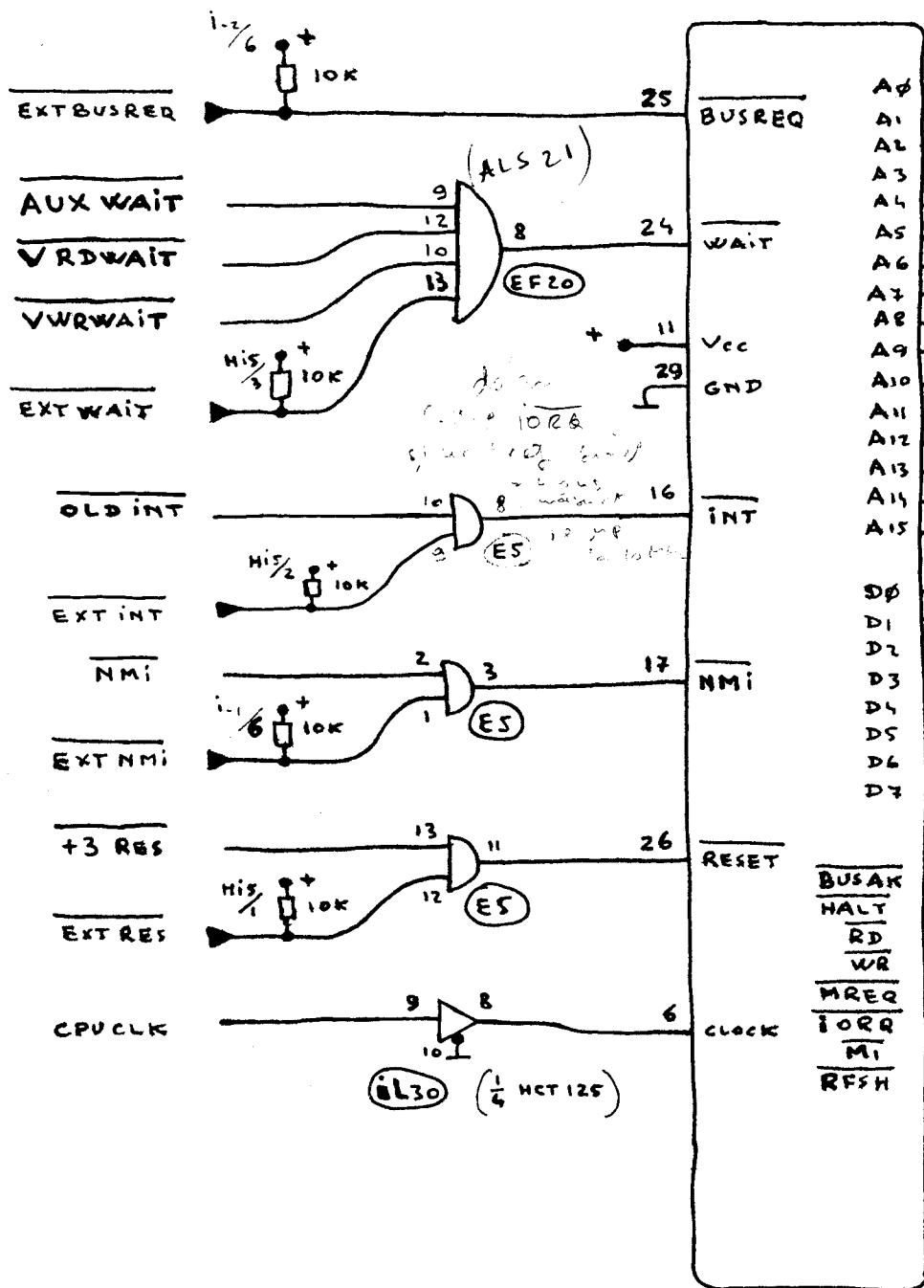


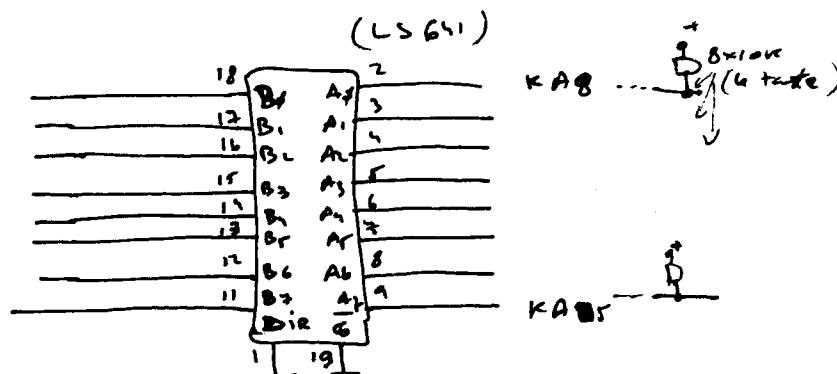
( Z 84 C 00 PEC )  
 Z 80 CPU



A <sub>0</sub>	→ A <sub>0</sub>
A <sub>1</sub>	→ A <sub>1</sub>
A <sub>2</sub>	→ A <sub>2</sub>
A <sub>3</sub>	→ A <sub>3</sub>
A <sub>4</sub>	→ A <sub>4</sub>
A <sub>5</sub>	→ A <sub>5</sub>
A <sub>6</sub>	→ A <sub>6</sub>
A <sub>7</sub>	→ A <sub>7</sub>
A <sub>8</sub>	→ A <sub>8</sub>
A <sub>9</sub>	→ A <sub>9</sub>
A <sub>10</sub>	→ A <sub>10</sub>
A <sub>11</sub>	→ A <sub>11</sub>
A <sub>12</sub>	→ A <sub>12</sub>
A <sub>13</sub>	→ A <sub>13</sub>
A <sub>14</sub>	→ A <sub>14</sub>
A <sub>15</sub>	→ A <sub>15</sub>
D <sub>0</sub>	↔ D <sub>0</sub>
D <sub>1</sub>	↔ D <sub>1</sub>
D <sub>2</sub>	↔ D <sub>2</sub>
D <sub>3</sub>	↔ D <sub>3</sub>
D <sub>4</sub>	↔ D <sub>4</sub>
D <sub>5</sub>	↔ D <sub>5</sub>
D <sub>6</sub>	↔ D <sub>6</sub>
D <sub>7</sub>	↔ D <sub>7</sub>

BUSAK	→ BUSAK
HALT	→ HALT
RD	→ RD
WR	→ WR
MREQ	→ MREQ
IORQ	→ IORQ
M1	→ M1
RFSH	→ RFSH

M 30 - 45



All address, data and RD, WR, MREQ, IORQ, M1, RFSH outputs have 10k pull up resistor each.